In the Claims

SUB D1 7

C1

26. (Amended) Memory circuitry comprising:

a semiconductor substrate;

a plurality of word lines received over the semiconductor substrate;

an insulative layer received over the word lines and the substrate, the insulative layer having at least one well formed therein, the well comprising a base received over the word lines, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area;

a plurality of memory cell storage capacitors received within the one well over the word lines; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

SUB D2 7

C2

33. (Amended) Memory circuitry comprising:

a semiconductor substrate;

an insulative layer received over the substrate, the insulative layer having at least one well formed therein, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area, the well having a substantially planar base;

a plurality of memory cell storage capacitors received within the one well, the memory cell storage capacitors respectively comprising a storage

Cond. C2

node container which is received partially within the insulative layer through the well base; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

Cancel claims 38-47.

Add new claims 48-53 as follows:

SUB E1

48. (Added) The memory circuitry of claim 26 wherein the insulative layer comprises SiO_2, and further comprising an Si_3N_4 comprising layer received on the well base.

C3

49. (Added) The memory circuitry of claim 48 wherein the Si_3N_4 comprising layer has a thickness of from about 40 Angstroms to about 125 Angstroms.

50. (Added) The memory circuitry of claim 48 wherein the Si_3N_4 comprising layer has a thickness of from about 50 Angstroms to about 70 Angstroms.

51. (Added) The memory circuitry of claim 33 wherein the insulative layer comprises SiO_2, and further comprising an Si_3N_4 comprising layer received on the well base.

52. (Added) The memory circuitry of claim 51 wherein the Si_3N_4 comprising layer has a thickness of from about 40 Angstroms to about 125 Angstroms.

53. (Added) The memory circuitry of claim 51 wherein the Si_3N_4 comprising layer has a thickness of from about 50 Angstroms to about 70 Angstroms.